

What is claimed is:

1 1. A method of executing instructions on a processor, the  
2 method comprising:

3 receiving a first condition code produced by  
4 executing a first instruction during a first clock cycle  
5 on an array of engines included in the processor;

6 receiving a second condition code produced by  
7 executing a second instruction during a second clock  
8 cycle on the array of engines included in the processor;  
9 and

10 executing a logical operator on the first and second  
11 condition codes during the second clock cycle on the  
12 array of engines included in the processor.

1 2. The method of claim 1, wherein executing the logical  
2 operator includes executing a logical "AND" operation.

1 3. The method of claim 1, wherein executing the logical  
2 operator includes ignoring the first condition code.

1 4. The method of claim 1, wherein executing the logical  
2 operator includes ignoring the second condition code.

1 5. The method of claim 1, wherein the first instruction is  
2 executed on one engine within the array of engines included in  
3 the processor.

1 6. The method of claim 1, wherein the first condition code  
2 indicates if the execution of the first instruction produced a  
3 numerical zero.

1 7. The method of claim 1, wherein the first condition code  
2 indicates if the execution of the first instruction produced  
3 an overflow.

1 8. The method of claim 1, wherein the first condition code  
2 includes data for determining a destination of a data packet.

1 9. The method of claim 1, wherein a third instruction is  
2 executed by the array of engines prior to executing the second  
3 instruction.

1 10. A computer program product, tangibly embodied in an  
2 information carrier, for executing instructions on a  
3 processor, the computer program product being operable to  
4 cause a machine to:

5 receive a first condition code produced by executing  
6 a first instruction during a first clock cycle on an  
7 array of engines included in the processor;

8 receive a second condition code produced by  
9 executing a second instruction during a second clock  
10 cycle on the array of engines included in the processor;  
11 and

12 execute a logical operator on the first and second  
13 condition codes during the second clock cycle on the  
14 array of engines included in the processor.

1 11. The computer program product of claim 10, wherein  
2 executing the logical operator includes executing a logical  
3 "AND" operation.

1 12. The computer program product of claim 10, wherein  
2 executing the logical operator includes ignoring the first  
3 condition code.

1 13. The computer program product of claim 10, wherein  
2 executing the logical operator includes ignoring the second  
3 condition code.

1 14. The computer program product of claim 10, wherein the  
2 first instruction is executed on one engine within the array  
3 of engines included in the processor.

1 15. The computer program product of claim 10, wherein the  
2 first condition code indicates if the execution of the first  
3 instruction produced a numerical zero.

1 16. The computer program product of claim 10, wherein the  
2 first condition code indicates if the execution of the first  
3 instruction produced an overflow.

1 17. The computer program product of claim 10, wherein the  
2 first condition code includes data for determining a  
3 destination of a data packet.

1 18. The computer program product of claim 10, wherein a third  
2 instruction is executed by the array of engines prior to  
3 executing the second instruction.

1 19. A packet classifier comprises:  
2 a process to receive a first condition code produced  
3 by executing a first instruction during a first clock  
4 cycle on an array of engines included in a processor;  
5 a process to receive a second condition code  
6 produced by executing a second instruction during a  
7 second clock cycle on the array of engines included in  
8 the processor; and

9           a process to execute a logical operator on the first  
10       and second condition codes during the second clock cycle  
11       on the array of engines included in the processor.

1       20. The packet classifier of claim 19, wherein executing the  
2       logical operator includes executing a logical "AND" operation  
3       to determine a destination for a packet.

1       21. The packet classifier of claim 19, wherein executing the  
2       logical operator includes ignoring the first condition code.

1       22. The packet classifier of claim 19, wherein executing the  
2       logical operator includes ignoring the second condition code.

1       23. The packet classifier of claim 19, wherein the first  
2       instruction is executed on one engine within the array of  
3       engines included in the processor.

1       24. The packet classifier of claim 19, wherein the first  
2       condition code indicates if the execution of the first  
3       instruction produced a numerical zero.

1       25. The packet classifier of claim 19, wherein the first  
2       condition code indicates if the execution of the first  
3       instruction produced an overflow.

1       26. The packet classifier of claim 19, wherein the first  
2       condition code indicates if the execution of the first  
3       instruction produced an overflow.

1       27. The packet classifier of claim 19, wherein a third  
2       instruction is executed by the array of engines prior to  
3       executing the second instruction.

1       28. A system comprising a processor capable of:

2           receiving a first condition code produced by  
3           executing a first instruction during a first clock cycle  
4           on an array of engines included in the processor;

5           receiving a second condition code produced by  
6           executing a second instruction during a second clock  
7           cycle on the array of engines included in the processor;  
8           and

9           executing a logical operator on the first and second  
10          condition codes during the second clock cycle on the  
11          array of engines included in the processor.

1   29. The system of claim 28, wherein executing the logical  
2   operator includes executing a logical "AND" operation.

1   30. The system of claim 28, wherein executing the logical  
2   operator includes ignoring the first condition code.

1   31. A system comprising:

2           a router including an input port for receiving data  
3           packets and an output port for data packet delivering as  
4           determined by a switch fabric; and

5           a processor capable of,

6           receiving a first condition code produced by  
7           executing a first instruction during a first clock  
8           cycle on an array of engines included in the  
9           processor,

10          receiving a second condition code produced by  
11          executing a second instruction during a second clock  
12          cycle on the array of engines included in the  
13          processor, and

14          executing a logical operator on the first and  
15          second condition codes during the second clock cycle  
16          on the array of engines included in the processor.

1 32. The system of claim 31, wherein executing the logical  
2 operator includes executing a logical "AND" operation.

1 33. The system of claim 31, wherein executing the logical  
2 operator includes ignoring the first condition code.

1 34. A processor comprising:

2 an engine having an instruction set including an  
3 instruction having a syntax that specifies a logical  
4 operation on a condition code determined by executing the  
5 instruction and on another condition code determined from  
6 a previously executed instruction.

1 35. The processor of claim 34, wherein the processor includes  
2 a second engine.

1 36. The processor of claim 34, wherein the engine is  
2 multithreaded.